WHAT IS CLAIMED IS:

1. A chip-type sensor against ESD and stress damages and contamination interference, the chip-type sensor comprising:

a substrate structure; and

a protection layer covering over the substrate structure, wherein the protection layer comprises, from bottom to top:

a first layer for providing a first stress against the substrate structure;

a second layer for providing a second stress against the substrate structure; and

a third layer for providing a third stress against the substrate structure, wherein the first stress and the third stress belong to one of a tensile stress and a compressive stress, and the second stress belongs to the other of the tensile stress and the compressive stress.

2. The chip-type sensor according to claim 1, wherein each of the first layer and the third layer is made of silicon dioxide, and the second layer is a single layer made of silicon nitride, silicon carbide, diamond-like carbon material or diamond material, or a composite layer having multiple layers each being made of silicon nitride, silicon carbide, diamond-like carbon material and diamond material.

3. The chip-type sensor according to claim 1, wherein the second layer is made of silicon dioxide, and each of the first layer and the third layer is a single layer made of silicon nitride, silicon carbide, diamond-like carbon material or

diamond material, or a composite layer having multiple layers each being made of silicon nitride, silicon carbide, diamond-like carbon material and diamond material.

4. The chip-type sensor according to claim 1, wherein the protection layer further comprises:

a polymeric material or ceramic atomic layer applied onto the third layer to provide a hydrophobic and lipophobic surface, which is to be in contact with a finger, so as to prevent a latent fingerprint from being formed thereon.

5. The chip-type sensor according to claim 4, wherein the polymeric material layer is made of Teflon or Teflon-like chemical structure material.

6. The chip-type sensor according to claim 4, wherein the polymeric material layer is formed on the third layer using a polymeric monomer solution having a plurality of monomers, each of which has a fluorocarbon (FC) polymer end and a polar silane group, the FC polymer end is exposed to protect an integrated circuit from external contamination, and the polar silane group is for firmly fixing the polymeric material layer to the third layer.

7. The chip-type sensor according to claim 6, wherein the FC polymer end has a soft fragment FC polymer bond.

8. The chip-type sensor according to claim 4, wherein the ceramic atomic layer is an aluminum oxide layer or a titanium oxide layer.

9. The chip-type sensor according to claim 1, wherein the protection layer has a thickness greater than 2 microns.

10. The chip-type sensor according to claim 1, wherein the protection layer has a thickness ranging from 3 to 5 microns.

11. The chip-type sensor according to claim 1, wherein the substrate structure comprises:

a silicon substrate having a plurality of sense circuits; and

a plurality of sense electrodes, which is arranged in an array on the silicon substrate, corresponds to the sense circuits, and electrically connected to the sense circuits, respectively.

12. The chip-type sensor according to claim 11, wherein the substrate structure further comprises:

a metal mesh crisscrossing between sense electrodes, being flush with the sense electrodes, and surrounding each of the sense electrodes, wherein the metal mesh is connected to a ground, and the protection layer completely covers over the metal mesh.

13. The chip-type sensor according to claim 12, wherein the substrate structure further comprises:

a plurality of ESD units connected to the metal mesh and formed between a predetermined number of adjacent sense electrodes among the sense electrodes, wherein the number of the ESD units is smaller than that of sense electrodes, and the protection layer partially covers over the ESD units.

14. The chip-type sensor according to claim 13, wherein the substrate structure further comprises:

a plurality of bonding pads serving as input/output portions of the chip-type sensor, wherein the protection layer partially covers over the bonding pads so as to form a plurality of first openings above the ESD units and a plurality of second openings above bonding pads, and a dimension of each of the first openings is smaller than that of each of the second openings.

15. The chip-type sensor according to claim 13, wherein a spacing between two adjacent ESD units substantially ranges from 500 to 1000 microns.

16. The chip-type sensor according to claim 11, wherein the sense electrodes comprise a plurality of sacrificial electrodes and a plurality of standard electrodes, the sacrificial electrodes are adjacent to the ESD units, respectively, and a dimension of each of the sacrificial electrodes is smaller than that of each of the standard electrodes.